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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/262,657	03/04/1999	SHUNPEI YAMAZAKI	SEL-126	9735

7590

12/16/2003

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EXAMINER

PRENTY, MARK V

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 12/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Advisory Action</b>	Application No. 09/262,657	Applicant(s) YAMAZAKI ET AL.	
	Examiner MARK V PRENTY	Art Unit 2822	

**--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

THE REPLY FILED 20 November 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

**PERIOD FOR REPLY** [check either a) or b)]

- a) ☒ The period for reply expires 4 months from the mailing date of the final rejection.
- b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
- ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on \_\_\_\_\_. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☐ The proposed amendment(s) will not be entered because:
- (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);
  - (b) ☐ they raise the issue of new matter (see Note below);
  - (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
  - (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: \_\_\_\_\_

3. ☒ Applicant's reply has overcome the following rejection(s): the 35 USC 112 rejection of claims 52, 54 and 56.
4. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☒ The a) ☐ affidavit, b) ☐ exhibit, or c) ☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. ☒ For purposes of Appeal, the proposed amendment(s) a) ☐ will not be entered or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: \_\_\_\_\_

Claim(s) objected to: \_\_\_\_\_

Claim(s) rejected: 1,2,4,5,7,8,10,11,13,14,30-42,44-47 and 49-56.

Claim(s) withdrawn from consideration: \_\_\_\_\_

8. ☐ The drawing correction filed on \_\_\_\_\_ is a) ☐ approved or b) ☐ disapproved by the Examiner.
9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). \_\_\_\_\_
10. ☐ Other: \_\_\_\_\_

*Mark V. Prenty*  
**Mark V. Prenty**  
 Primary Examiner

Continuation of 5. the applicant's arguments are without merit and do not squarely and fully address any of the rejections.

First, the applicant's argument: "However, Saraswat et al. do not consider that the off current of silicon germanium is higher than the off current of silicon. Therefore, it is improper to combine Zhang et al. '733 and Saraswat et al., since Saraswat et al. do not teach the appropriate use of silicon and silicon germanium," is without merit, because it ignores the manner in which Zhang et al. '733 and Saraswat et al. have been combined in that 35 USC 103 rejection (i.e., "Zhang '733's semiconductor device is an active-matrix circuit. The first thin film transistor having a first active layer 26a is part of a peripheral driver circuit and the second thin film transistor having a second active layer 26b is part of the matrix region. The difference between Zhang '733's semiconductor device and claim 1's semiconductor device is Zhang '733's first thin film transistor's active layer comprises silicon while claim 1's first thin film transistor's active layer comprises Si1-xGex where  $0 < x < 1$ . Saraswat teaches forming an active-matrix circuit's peripheral driver transistors from Si1-xGex where  $0 < x < 1$  instead of silicon, because the resulting transistors have significantly improved electrical characteristics, such as higher mobility (see the entire patent, particularly column 1, lines 20-58, and column 2, lines 19-43). It would have been obvious to one skilled in this art to form Zhang '733's first thin film transistor's active layer 26a of Si1-xGex where  $0 < x < 1$  instead of silicon, in order to improve that driver circuit transistor's electrical characteristics, as taught by Saraswat."). In this regard, note that Zhang et al. '733 disclose that an active-matrix circuit's pixel and driver transistors require low leakage and high speed, respectively (see Zhang et al. '733's Background of the Invention, for example), and that the application of Saraswat et al.'s high speed SiGe driver transistor teaching to Zhang et al. '733's driver transistor is consistent therewith. Accordingly, Zhang et al. '733 together with Saraswat et al. clearly "teach the appropriate use of silicon and silicon germanium" for an active-matrix circuit's pixel and driver thin film transistors, respectively (i.e., Zhang et al. '733 disclose forming an active-matrix circuit's pixel transistor of certain silicon for low leakage and Saraswat et al. teach forming an active-matrix circuit's driver transistor of silicon germanium for high speed).

Furthermore, the applicant's argument: "Zhang et al. '733 disclose that it is necessary that the TFTs used in the peripheral circuit and the TFTs used in the pixel circuit are formed on the same substrate at the same time," does not appear to be germane because the applicant fails to explain how such is relevant to, let alone rebuts, the rejections. Such is without merit in any event because Zhang et al. '733 disclose forming differently tailored pixel and driver transistors on the same substrate at the same time by varying one parameter (see the entire patent, including column 4, lines 35-43), and Saraswat et al.'s SiGe driver transistor teaching is consistent therewith.

*Mark V. Prenty*  
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